21. The system of claim 1, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

22. The system of claim 1, wherein:

the cache memory comprises an address cache and a data cache.

23. The apparatus of claim 6, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

24. The apparatus of claim 6, wherein:

the cache memory comprises an address cache and a data cache.

REMARKS

Claims 1-3 and 6-8 have been rejected under 35 USC 102(e) as being anticipated by U.S. patent no. 6,263,398 ("Taylor").

Claims 1-2, 6-7 and 21-24 have been rejected under 35 USC 102(e) as being anticipated by U.S. patent no. 6,288,923 ("Sakamoto").

Claim 5 has been rejected under 35 USC 103(a) as being unpatentable over Sakamoto, or alternatively over Taylor.

Claims 4 and 9 have been rejected under 35 USC 103(a) as being unpatentable over Sakamoto in view of U.S. patent no. 6,347,055 ("Motomura"), or alternatively in over Taylor in view of Motomura.

Applicants respectfully traverse these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Independent claim 1 recites a cache memory, on the same integrated circuit as the main memory, that may simultaneously contain multiple addresses representing data requested from the main memory. Support for this limitation is shown throughout the disclosure, including paragraph 0022. Neither Taylor nor Sakamoto disclose these limitations. The cache memory of Taylor is limited to storing a single address at a time, that being the address of the page that is stored in the cache memory.

Claims 2-5 and 21-22 depend from claim 1 and therefore contain the same limitations not disclosed or suggested by the cited references.

Independent claim 6 recites a cache memory, on the same integrated circuit as the main memory, that stores data from non-consecutive main memory addresses in adjacent locations in cache. For example, in an embodiment having a cache to store four quadwords, each quadword might have an address that is not consecutive with the adjacent quadwords (see paragraphs 0022, 0028). Neither Taylor nor Sakamoto discloses or suggests this.

Claims 7-9 and 23-24 depend from claim 6 and therefore contain the same limitations not disclosed or suggested by the cited references.

Regarding claims 4 and 9, they depend from claims 1 and 6, respectively, and contain the same limitations as claims 1 and 6. Motomura does not disclose or suggest the limitations that are missing from Taylor and Sakamoto

CONCLUSION

For the foregoing reasons, Applicant submits that claims 1-9 and 21-24 are now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. No fee is believed due in connection with this response. If this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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APPENDIX A

Marked-up version of amended claims

1. (Amended twice) A system comprising:

a processor; and

a memory device coupled to the processor and contained within a single integrated circuit, the memory device including:

a main memory; and

a cache memory coupled to the processor and to the main memory to simultaneously contain multiple addresses representing data [store data from non-consecutive addresses] requested from the main memory.

6. (Amended twice) An apparatus comprising:

a memory device to couple to a processor through a bus, the memory device including on a single integrated circuit:

a main memory; and

a cache memory coupled to the main memory to store data in adjacent locations in the cache memory from non-consecutive addresses requested from the main memory.